

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

This listing will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A processor power-saving control method which employs a plurality of OSs whose execution is controlled by a processor, wherein said plurality of OSs include

a primary OS for receiving a timer interrupt issued from a hardware timer after a predetermined time lapse, and

a secondary OS treated as a task to be executed by said primary OS, said processor power-saving control method comprising the steps of:

upon receiving said timer interrupt, determining with said primary OS whether there exists any task to be ~~executed, this step being performed said primary OS~~ executed; and

when the primary OS determines there exists any task to be executed on said secondary OS, interrupting said secondary OS by issuing a secondary-OS interrupt from the primary OS to the secondary OS.

Claim 2 (Currently Amended): A processor power-saving control method which employs a plurality of OSs whose execution is controlled by a processor,

operation of said processor being stopped when there exists no task to be executed on said plurality of OSs,

said processor power-saving control method controlling timer interrupt processing performed by a hardware timer which activates said processor after an arbitrary time lapse,

said processor power-saving control method keeping a power-saving state of said processor,

said plurality of OSs including a primary OS for receiving a timer interrupt issued from said hardware timer and a secondary OS treated as a task to be executed by said primary OS,

~~wherein~~ said processor power-saving control method ~~comprises~~ comprising: a primary-OS process step performed by said primary OS, OS; a secondary-OS process step performed by said secondary OS, OS; and a secondary-OS interrupt step,

said primary-OS process step including [[:]]

~~a step of~~ detecting said timer ~~interrupt~~; interrupt,

a first determination step of, upon receiving said timer interrupt, determining whether there exists any task to be ~~executed~~; executed, and

a processor stopping step of, when there is no task to be executed, stopping said processor;

said secondary-OS process step including [[:]]

a second determination step of determining whether there exists any task to be ~~executed~~; executed, and

~~a step of~~, when there is no task to be executed, handing over processing to said first determination step;

said secondary-OS interrupt step including

receiving a secondary-OS interrupt from said primary OS,

~~whereby~~ when said first determination step has determined that there exists any task to be executed on said secondary OS, ~~said secondary-OS interrupt step~~ performs performing interrupt processing on said secondary OS, and

~~executes~~ executing said second determination step at a predetermined time measured from said interrupt.

Claim 3 (Original): The processor power-saving control method as claimed in claim 2, wherein said secondary-OS interrupt step is executed by a periodically-activating handler which interrupts said secondary OS at regular time intervals.

Claim 4 (Original): The processor power-saving control method as claimed in claim 2, wherein said secondary-OS interrupt step is executed by an alarm handler which interrupts said secondary OS after a specified time period.

Claim 5 (Original): The processor power-saving control method as claimed in claim 2, wherein said secondary-OS interrupt step is executed by a high-priority task which is a task for interrupting said secondary OS and has a highest priority order among tasks to be executed by said primary OS.

Claim 6 (Original): The processor power-saving control method as claimed in claim 2, wherein said processor stopping step includes a step of determining whether time taken until said hardware timer issues a next timer interrupt is longer than a predetermined time, and if a measured time is longer than said predetermined time, said processor stopping step stops operation of said processor.

Claim 7 (Original): The processor power-saving control method as claimed in claim 2, wherein said primary-OS process step further comprises steps of:

when said hardware timer periodically performs timer interrupt processing at regular time intervals, determining whether timer interrupt processing is required again by a time at which a task is to be executed; and

if timer interrupt processing is not required again, stopping said hardware timer.

Claim 8 (Original): The processor power-saving control method as claimed in claim 7, wherein said primary-OS process step further comprises a step of:

detecting a timer interrupt issued by a long-periodic hardware timer which issues a timer interrupt at a time interval longer than that of said hardware timer.

Claim 9 (Original): The processor power-saving control method as claimed in claim 2, wherein said primary-OS process step further comprises a step of:

detecting a timer interrupt issued by a time-of-day timer which measures a time of day as well as issuing a timer interrupt at a predetermined time of day.

Claim 10 (Currently Amended): A computer readable storage medium storing a plurality of OSs whose execution is controlled by a processor which is stopped when there exists no task to be executed, said plurality of OSs including a primary OS for receiving a timer interrupt issued from a hardware timer which activates said processor after an arbitrary time lapse, and a secondary OS treated as a task to be executed by said primary OS,

wherein said computer readable storage medium stores a program which causes a computer to perform a primary-OS process step on said primary OS, a secondary-OS process step on said secondary OS, and a secondary-OS interrupt step,

said primary-OS process step including [[:]]

~~a step of~~ detecting a timer interrupt issued by said hardware ~~timer~~; timer,

a first determination step of, upon detecting said timer interrupt, determining whether there exists any task to be ~~executed~~; executed, and

a processor stopping step of, when there is no task to be executed, stopping said processor;

said secondary-OS process step including [[:]]

a second determination step of determining whether there exists any task to be ~~executed~~; executed, and

~~a step of~~, when there is no task to be executed, handing over processing to said first determination step;

said secondary-OS interrupt step including

receiving a secondary-OS interrupt from said primary OS,

~~whereby~~ when said first determination step has determined that there exists any task to be executed on said secondary OS, ~~said secondary-OS interrupt step performs~~ performing interrupt processing on said secondary OS, and

~~executes~~ executing said second determination step at a predetermined time measured from said interrupt.

Claim 11 (Currently Amended): A processor power-saving control device comprising:

timer means including a hardware timer for issuing a timer interrupt after an arbitrary time lapse, and activating a processor, operation of said processor being stopped when there exists no task to be executed; and

storage means for storing a primary OS and a secondary OS;

wherein said primary OS, upon receiving said timer interrupt, ~~said primary OS determines~~ is configured to determine whether there exists any task to be executed, and ~~stops~~

to stop said processor if there is no task to be ~~executed~~, executed ~~or issues~~ and to issue an a
secondary-OS interrupt if there is any task to be executed; and

~~wherein~~ said primary OS, upon receiving ~~an~~ the secondary-OS interrupt from said
primary OS, ~~said secondary OS determines~~ is configured to determine whether there exists
any task to be executed, and if there is any task to be executed, ~~said secondary OS executes~~
to execute the task, said secondary OS being treated as a task to be executed by said primary
OS.

Claim 12 (Original): The processor power-saving control device as claimed in claim
11, wherein said timer means has a long-periodic timer which issues a timer interrupt at a
time interval longer than that of said hardware timer.

Claim 13 (Original): The processor power-saving control device as claimed in claim
11, wherein said timer means has a time-of-day timer.

Claim 14 (New): The processor power-saving control method of claim 1, further
comprising the step of:

activating the secondary OS from a sleep mode in response to the secondary OS
receiving the secondary-OS interrupt issued from the primary OS.

Claim 15 (New): The process power-saving control method of claim 2, wherein the
secondary-OS interrupt step further includes the step of:

activating the secondary OS from a sleep mode in response to the secondary OS
receiving the secondary-OS interrupt from the primary OS.

Claim 16 (New): The computer readable storage medium of claim 10, wherein the secondary-OS interrupt step includes the step of:

activating the secondary OS from a sleep mode in response to the secondary OS receiving the secondary-OS interrupt from the primary OS.

Claim 17 (New): The processor power-saving control device as claimed in claim 11, wherein said secondary OS is further configured to activate from a sleep mode in response to the receipt of the secondary-OS interrupt.